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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,081	ASANO ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *7 and 8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

This application contains claims 7 and 8 drawn to an invention nonelected with traverse in the reply filed 2/24/2005. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4-6, 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as obvious over Nagao et al. (US PGPub 2001/0053559, hereinafter Nagao).

Regarding claim 1, Figures 1 and 4 of Nagao discloses a semiconductor device having a thin film resistance element 111 through an interlayer insulating film (110 or 403) above an area where a wire (107 or 401) is formed on a semiconductor substrate (100 or 400), wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects to the surface of the semiconductor substrate. Note that pixel electrode 111 inherently has a resistance and therefore can be considered a resistance element. Also note that Nagao discloses the device shown in Figure 1 is formed using the principles shown in Figure 4

(paragraph [0030]), so it also has the step and tapered angle shown in Figure 4. Nagao does not specifically disclose that the taper angle is 10 degrees or less. However, Nagao does disclose it is desirable to improve the flatness (paragraphs [0016] and [0033]). This is supported by the fact that Figure 1 appears to show the insulating film 110 has a completely flat surface. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nagao by using a taper angle less than 10 degrees, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 2, Figure 1 of Nagao discloses the interlayer insulating film 110 comprises an inorganic spin-on-glass (SOG) film (paragraph [0031]) formed so as to cover the overall area below the area where the thin film resistance element is formed.

Regarding claim 4, Figure 1 of Nagao discloses the thin film resistance element 111 is formed on an area where the wire 107 is formed. Figure 4 of Nagao discloses a wire interval of 5-300 microns (based on subtracting "L" from "P", paragraph [0018]), although it is not clear if the same spacing is used for the wires 107 and 108 shown in the device of Figure 1. Therefore, it appears Nagao does not specifically disclose the wire interval is 1.7 microns or more. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the claimed wiring interval, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 5, Figure 1 of Nagao discloses the thin film resistance element 111 is formed above the area where the wire 107 is formed, and the thin film resistance element and the

wire are disposed in parallel to each other so that the projections thereof are overlapped with each other. Note the pixel electrode 111 inherently extends in more than one direction. For instance, looking at Figure 1, the electrode 111 also extends into the page, making it parallel to the wire 107. Alternatively, it can be considered that electrode 111 is parallel to wire 107 in the sense that 111 is parallel to the width direction of the wire 107.

Regarding claim 6, Figure 1 of Nagao discloses a thin film resistance element 111 through an interlayer insulating film 110 above an area where a wire 107 is formed, wherein the insulating film comprises an inorganic SOG film (paragraph [0031]) formed so as to cover the overall area below an area where the thin film resistance element is formed.

Regarding claim 9, the claim is essentially a combination of claims 1, 2, and 4. Therefore, the above rejections regarding those claims similarly apply.

Regarding claim 10, Nagao does not specifically disclose the resistance element has a width between 1 and 10 microns and a thickness between 10 and 50nm. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Nagao by using the claimed ranges, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 12, the claim is essentially a combination of claims 1, 2, and 4. Therefore, the above rejections regarding those claims similarly apply. The only difference is that claim 12 recites a plurality of wires. Figure 1 of Nagao discloses a plurality of wires formed on a semiconductor substrate.

Claims 1, 3, 6, and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiiki et al. (US PGPUB 2002/0020879, hereinafter Shiiki) in view of Nagao.

Regarding claim 1, Figure 1A of Shiiki discloses a semiconductor device having a thin film resistance element 2 through an interlayer insulating film 3 above an area where a wire (4 or 6) is formed on a semiconductor substrate. Shiiki does not specifically disclose a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the thin film resistance element is formed intersects to the surface of the semiconductor substrate is set to 10 degrees or less. Figure 4 of Nagao discloses a method of forming an interlayer insulating film 403 over wires 401, wherein the upper surface of the insulating film has a small step. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Shiiki by using the method of Nagao for the purpose of obtaining a relatively flat surface (paragraph [0033] of Nagao) without requiring any additional planarization steps, such as CMP. Note that Shiiki discloses using CMP to flatten the interlayer insulating film (see abstract). It is known in the art that CMP has many drawbacks, including high cost. Therefore, eliminating that step would reduce the cost and simplify the production process. A further difference between Shiiki and the claimed invention is the taper angle is less than 10 degrees. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify Shiiki and Nagao by using a taper angle less than 10 degrees, since it has been

held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 3, since the step in the insulating film is formed as a result of the underlying wiring 6, and that wiring is located under the resistance element, it follows that an upper surface of the interlayer insulating film has a higher area adjacent to an area where the thin film resistance element is formed than in an area where the resistance element is not formed (see Figures 1A and 1B of Shiiki). It is further obvious to use the inorganic SOG film of Nagao (paragraph [0031]) for the purpose of using an insulating material that can function as a good leveling film.

Regarding claim 6, Figure 1A of Shiiki discloses a thin film resistance element 2 through an interlayer insulating film 3 above an area where a wire 4 is formed, wherein the film is formed to cover the overall area below an area where the thin film resistance element is formed. It is obvious to use the inorganic SOG film of Nagao (paragraph [0031]) for the purpose of using an insulating material that can function as a good leveling film.

Regarding claims 9 and 12, the rejection of claims 1 and 3 set forth above similarly applies to these claims. Regarding claim 12, Figure 1A of Shiiki discloses a plurality of wires 4. A further difference between Shiiki and the claimed invention is a wire interval is set to 1.7 microns or more. It would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the invention of Shiiki by using the claimed wire interval range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

In re Aller, 105 USPQ 233. It would have been obvious to use a wire interval of 1.7 microns or more to reduce the parasitic capacitance between the wires.

Regarding claims 10 and 11, Shiiki discloses the thin film resistance element 2 is formed to have a thickness of 500 angstroms (50nm) (paragraph [0052]), which is within the claimed range of 10-50 nm. Shiiki does not specifically disclose the resistance element has a width between 1 and 10 microns. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the invention of Shiiki by using the claimed width range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Response to Arguments

Applicant's arguments filed August 19, 2005 have been fully considered but they are not persuasive.

Applicant argues that "according to Nagao *et al.*, element 11 is a pixel electrode" and therefore Nagao does not disclose a resistor. The Examiner addressed this distinction in the original rejection. As stated previously, the pixel electrode inherently has at least some resistance, and therefore can be considered a resistor. Applicant has not specifically defined the term "resistor" in a manner that would preclude this interpretation.

Applicant argues that, "In the publication of Shiiki *et al.*, the interlayer film is flattened and located in the active region. However, the present invention provides the unexpected and

superior result of permitting formation of the resistor without the flattening process. Such superior results rebut the examiner's conclusion that one skilled in the art would be motivated to modify the apparatus of Shikki *et al.*". This argument is not understood. First of all, the claims do not state that the device is formed without a flattening process. Secondly, the point of the above 103 rejection was to modify Shiiki by eliminating the flattening process (CMP). Nagao discloses obtaining a flat interlayer insulation film without using CMP. As stated in the above rejection, the problems associated with a CMP process are well known in the art. Therefore the benefits of eliminating such a step would hardly be unexpected. Further, Applicant has not specifically stated what the unexpected and superior results are. Simply stating that the claimed invention provides unexpected and superior results in not sufficient to overcome a 103 rejection. Applicant must provide evidence to support this allegation. Applicant further argues that, "In response to the examiner's assertion that this range is a result-effective variable, the applicant's point out the unexpected and superior results achieved by such a range discussed above". Once again, Applicant must provide evidence to support this allegation of unexpected and superior results. It should be noted that the claimed range is essentially provides that the interlayer insulating film is flat, but not completely flat. If it were completely flat, the angle would be 0 degrees. The device of Nagao is clearly not completely flat (as shown in Figure 4), but it would certainly be obvious modify Nagao to have the surface as flat as possible (i.e., less than 10 degrees). The benefits of obtaining a flat surface would not be unexpected as apparently alleged by Applicant.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Matthew C. Landau

October 28, 2005